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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,779	GOPALAKRISHNAN ET AL.	
	Examiner	Art Unit	
	Sarah K. Salerno	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _23 October 2007_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-43_ is/are pending in the application.

4a) Of the above claim(s) _40-42_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-39 and 43_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _17 December 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _04/04/05_.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant’s election without traverse of Group 1, Claims 1-39, 43 in the reply filed on 10/23/07 is acknowledged.

2. Claims 40-42 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method of manufacturing, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10/23/07.

Applicant's election with traverse of Species 1 in the reply filed on 10/23/07 & 01/30/08 is acknowledged. The traversal is on the ground(s) that the claims are linked as to form a single general inventive concept and therefore the species restriction has insufficient basis. Applicant’s arguments are persuasive and claims 1-39 &43 will be examined,

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 8-9, 38-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 38-39 contains the limitation “first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite

polarization" which is unclear in describing the first and second regions. The claim is being interpreted as the first and second junction are of opposite conduction types (i.e. n and p).

Claim 8 & 9 contains the term preponderantly which means superior in weight, force or influence which does not match the context in which it is used in claim 8 & 9. The claims are being interpreted as the gate being located over the second region for claim 8 and over the intermediate region for claim 9.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-20 & 38-39 and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Burr (US Patent 5,985,727).

Claim 1: Burr teaches a semiconductor device, comprising: a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and a gate capacitively-coupled to the body and adapted for using a control signal, when the body is reversed biased, to modulate the length of the

intermediate region by changing a concentration of carriers in the intermediate region (Fig 1, Col. 6-8).

Claim 2: Burr teaches the gate is further adapted to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state (Col. 4, 6-10).

Claim 3: Burr teaches means for modulating an electric field within the body to cause the device to transition between a current- conducting state in which the device is in avalanche breakdown condition and a current-blocking state (Col. 4, 6-10).

Claim 4: Burr teaches a relatively high bias voltage at the gate maintains the device in a current-conducting state in which the device is in an avalanche breakdown condition, and wherein a relatively low bias voltage at the gate maintains the device in a current-blocking state (Col. 4, 6-10).

Claim 5: Burr teaches the relatively high bias voltage shortens the effective length of the intermediate region (Col. 4, 6-10).

Claim 6: Burr teaches a relatively low bias voltage at the gate maintains the device in a current-conducting state in which the device is in an avalanche breakdown condition, and a relatively-high bias voltage at the gate maintains the device in a current-blocking state (Col. 4, 6-10).

Claim 7: Burr teaches the relatively low bias voltage shortens the effective length of the intermediate region (Col. 4, 6-10).

Claim 8: Burr teaches the gate is located at least preponderantly over the second region (Col. 4, 6-10).

Claim 9: Burr teaches the gate is located at least preponderantly over the intermediate region (Col. 4, 6-10).

Claim 10: Burr teaches the gate is located to provide a surface channel nearer the second junction than the first junction (Col. 4, 6-10).

Claim 11: Burr teaches wherein when the body is reversed- biased, the first region is maintained at a relatively lower voltage level than the second region, the difference in potential of the first and second regions being sufficient to cause a breakdown condition in the intermediate region in response to the control signal modulating the length of the intermediate region and thereby reducing the distance across the intermediate region over which the potential drops (Col. 4, 6-10).

Claim 12: Burr teaches the intermediate region has a polarity that is neutral relative to the polarity of the first and second regions (Col. 8).

Claim 13: Burr teaches the intermediate region is lightly doped to achieve the polarization of one of the first and second regions, the intermediate region having a substantially lower dopant concentration level, relative to said one of the first and second regions (Col. 8).

Claim 14: Burr teaches the intermediate region is substantially intrinsic (Col. 8).

Claim 15: Burr teaches the gate is further adapted to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state in which substantially no leakage current passes between the first and second regions (Col. 4, 6-10).

Claim 16: Burr teaches a controller coupled to the gate and adapted for applying the control signal to change the concentration of carriers in the intermediate region (Col. 12).

Claim 17: Burr teaches the gate is further adapted to increase an electric field in the intermediate region and for causing an avalanche breakdown condition (Col. 4, 6-10).

Claim 18: Burr teaches A semiconductor device comprising: a multi-region body including a P-type region, an N-type region and an intermediate region having a first junction with the P-type region and a second junction with the N-type region, the body adapted to be reverse biased across the P-type and N- type regions; a gate coupled via an intervening gate dielectric material to the intermediate region, and offset to present an electric field substantially at only one of the two junctions; and the gate, the P-type region and the N-type region being adapted and controllable to switch the device between at least two stable conductance states in response to a voltage-bias control signal applied to the gate (Fig. 1; Col. 4, 6-10).

Claim 19: Burr teaches the device is switched between a high-resistance conductance state and a low-resistance conductance state as a function of an avalanche breakdown condition at a field-induced junction in the intermediate region (Col. 4, 6-10).

Claim 20: Burr teaches the intermediate region has a length that separates the first and second junctions sufficiently to permit the avalanche breakdown condition before another breakdown condition when the body is reverse biased (Col. 4, 6-10).

Claim 38: Burr teaches a semiconductor device comprising: a relatively thin intermediate region defined by sides including an upper portion and a sidewall portion; a first region dominated by a first polarization that extends to a first junction with the intermediate region; a second region dominated by a second polarization that extends to a second junction with the intermediate region; and a gate extending around and capacitively coupled to at least two sides of the intermediate region for coupling a voltage to the intermediate region, when the first and second regions are reversed biased, to present an electric field substantially at only one of the first and second junctions, the device responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes through the intermediate region (Fig. 1; Col. 4, 6-10).

Claim 39: Burr teaches a semiconductor device, comprising: a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and means for presenting, when the body is reversed biased, an electric field at the first junction, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body (Fig. 1; Col. 4, 6-10).

Claim 43: A semiconductor device, comprising: a multi-region body having an upper surface and including a first region dominated by a first polarization that extends

to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having an upper portion over a lower portion and a length extending from the first junction to the second junction; a gate capacitively-coupled to the body and adapted for using a control signal, when the body is reversed biased, to modulate the length of the intermediate region by changing a concentration of carriers in the intermediate region and thereby causing the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state; and the avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state (Fig. 1; Col. 4, 6-10)..

7. Claims 21-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Goo (US Patent 5,677,215).

Claim 21: Goo teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and a gate coupled to the body via an intervening dielectric material and offset for using a control signal, when the body is reversed biased, to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable

conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body (FIG. 4; Col. 3-4).

Claim 22: Goo teaches the body and the gate are adapted to access data stored at the data storage node as a function of the avalanche breakdown condition (FIG. 4; Col. 3-4).

Claim 23: Goo teaches the body and the gate are adapted to read data from the data storage node as a function of the avalanche breakdown condition (FIG. 4; Col. 3-4).

Claim 24: Goo teaches the body and the gate are adapted to write data to the data storage node as a function of the avalanche breakdown condition (FIG. 4; Col. 3-4).

Claim 25: Goo teaches a charge at the data storage node is maintained by controlling the body in a reverse biased condition (FIG. 4; Col. 3-4).

Claim 26: Goo teaches the body and the storage node are adapted to drain a charge at the storage node in response to the body being placed in a forward biased condition (FIG. 4; Col. 3-4).

Claim 27: Goo teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and a gate coupled to the body via an intervening

dielectric material and offset for using a control signal, when the body is reversed biased, to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes through the body as a function of a charge at the data storage node (FIG. 4; Col. 3-4).

Claim 28 Goo teaches the data storage node is coupled to the gate, the gate responding to a charge at the data storage node by presenting the electric field (FIG. 4; Col. 3-4).

Claim 29: Goo teaches a sense device coupled to the body and adapted to detect data stored at the data storage node in response to current passing through the body (FIG. 4; Col. 3-4).

Claim 30: Goo teaches a memory circuit comprising: a data storage node; first and second multi-region bodies, each body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; a first gate coupled to the first body via an intervening dielectric material and offset for using a control signal, when the first body is reversed biased, to present an electric field substantially at only one of the first and second junctions of the first body, the first body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the first body is in an avalanche breakdown condition and current passes between the

data storage node and the first body; and a second gate coupled to the data storage node and to the second body via an intervening dielectric material and adapted for using a charge at the data storage node, when the second body is reversed biased, to modulate an electric field in the intermediate region of the second body, the second body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the second body is in an avalanche breakdown condition and current passes through the second body (FIG. 4; Col. 3-4).

Claim 31: Goo teaches a sense device coupled to the second body and adapted to detect data as a function of sensed current passing through the second body, and wherein the second gate is further adapted to influence an electric field substantially at only one of the first and second junctions (FIG. 4; Col. 3-4).

Claim 32: Goo teaches a semiconductor device, comprising: a multi-region body including a first region dominated by a first polarization that extends to a first junction, a second region dominated by an opposite polarization that extends to a second junction, and an intermediate region having a length extending from the first junction to the second junction; and first and second gates coupled to the body via intervening dielectric material and adapted for using control signals, when the body is reversed biased, to present an electric field at one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition (FIG. 4; Col. 3-4).

Claim 33: Goo teaches the first gate is adapted to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, the body being held in a steady state without the avalanche breakdown condition occurring absent a similarly-biased control signal capacitively coupled to the body from the second gate (FIG. 4; Col. 3-4).

Claim 34: Goo teaches the first gate is adapted to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, the body switching to the current-conducting state in response to a second voltage-bias control signal being capacitively coupled to the body, the first and second voltage-bias control signals being of similar bias (FIG. 4; Col. 3-4).

Claim 35: Goo teaches the second gate is responsive to temperature and adapted to apply a control signal to the body that counters temperature-related effects that alter the creation of the avalanche breakdown condition in response to a control signal being applied by the first gate (FIG. 4; Col. 3-4).

Claim 36: Goo teaches the second gate is adapted to apply the control signal to maintain a threshold voltage level in the intermediate region, the threshold voltage being a minimum amount of additional voltage applied to the intermediate region for causing the avalanche breakdown condition (FIG. 4; Col. 3-4).

8. Claim 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Armstrong (US Patent 4,062,699).

Claim 37: Armstrong teaches an inverter circuit comprising: first and second multi-region bodies, each body having a highly-doped P-type region that extends to a first junction, a highly-doped N-type region that extends to a second junction, and an intermediate region having a neutral polarity relative to the P- type and N-type regions and having a length extending from the first junction to the second junction, the N-type region of the first body and the P-type region of the second body being coupled to a common output node; first and second gates respectively capacitively coupled to the first and second bodies and each adapted, when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions; and an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node (Fig. 5a, Col. 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./
Examiner, Art Unit 2814

/Theresa T. Doan/
Primary Examiner, Art Unit 2814